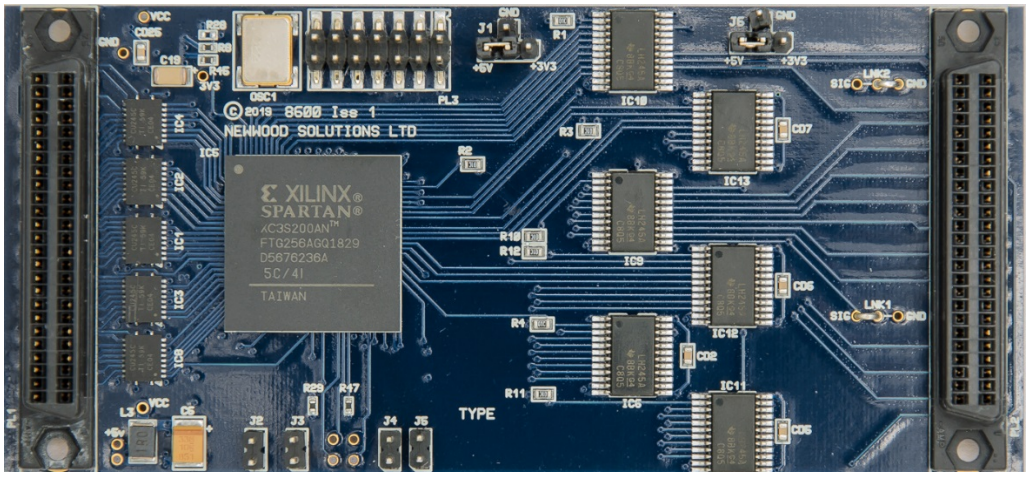
sales@newwoodsolutions.co.uk
www.newwoodsolutions.co.uk

DIO8600 Reconfigurable FPGA with 48-bit DIGITAL I/O IndustryPack®



Product Description
This is a single-width IP module with user configurable FPGA in the form of a Xilinx Spartan 3 FPGA XC3S200AN-5 with 200,000 system gates, and forty eight channels of buffered digital input/output. The 48 digital I/O lines can be programmable as inputs or outputs with a resistor network which allows a selectable pull up/down voltage of GND, +3.3V or 5V). The unit also has an onboard 50MHz clock oscillator. The FPGA logic is configurable via JTAG plug on the IP card.

XC3S200AN	
System Gates	200K
Logic Cells	4,032
Dedicated Multipliers	16
Block RAM Blocks	16
Block RAM Bits	288K
Distributed RAM Bits	28K
Flash Size Bits	4M
User Flash Bits	2M
DCMs	4

PRODUCT SPECIFICATIONS

Size:	Single width Industry Pack 1.8ins x 3.9 ins
Operating temp:	0 to 45 deg C ambient
Number of input/outputs:	48 (configurable as 6 groups of 8 in or 8 out)
Input level:	TTL
Output level	TTL 24mA, programmable logic sense high or low true
Input/output termination:	4k7 ohms to 0V, or +3.3V or 5V by jumper selection
Internal clock:	50MHz oscillator.
Clock accuracy:	+/-100ppm (0.01%)
Power:	+5V @ 250mA typical

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Registration Number: 10514548 VAT Number: GB 257 7693 51

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IP8600 Board I/O Pin Assignments 50-way SCSI-2 connectors

TB8304 is a VME rear transition card with 4 x 50-way SCSI-2 connectors each which can be connected to an 8901 terminal board via 50-way SCSI-2 cable.

DIO8600 Signal	DIO8600 Buffer IC PCB IDENT	DIO8600 FPGA Pinning	DIO8600 50-way SCSI-2 Pinning		VTB8304 50-way SCSI-2 Pinning	VDB8901 Terminal Board	Notes
Set I/O direction Bank 1 FPGA Pin = K15 J6 controls selection of I/O termination voltage							
I/O	12	C8	2		1	1	
I/O	12	D8	4		2	2	
I/O	12	C10	6		3	3	
I/O	12	D9	8		4	4	
I/O	12	K16	10		5	5	
I/O	12	J16	12		6	6	
I/O	12	J14	14		7	7	
I/O	12	H14	16		8	8	
Set I/O direction Bank 2 FPGA Pin = G14 J6 controls selection of I/O termination voltage							
I/O	11	F8	18		9	9	
I/O	11	E7	20		10	10	
I/O	11	C6	22		11	11	
I/O	11	D7	24		12	12	
I/O	11	E10	26		13	13	
I/O	11	D10	28		14	14	
I/O	11	D11	30		15	15	
I/O	11	C12	32		16	16	
Set I/O direction Bank 3 FPGA Pin = G16 J6 controls selection of I/O termination voltage							
I/O	13	F16	34		17	17	
I/O	13	F14	36		18	18	
I/O	13	C15	38		19	19	
I/O	13	B8	40		20	20	
I/O	13	H16	42		21	21	
I/O	13	H15	44		22	22	
I/O	13	F15	46		23	23	
I/O	13	E16	48		24	24	
Set I/O direction Bank 4 FPGA Pin = L16 J1 controls selection of I/O termination voltage							
I/O	6	D13	1		26	26	
I/O	6	C13	3		27	27	
I/O	6	B15	5		28	28	
I/O	6	B14	7		29	29	
I/O	6	A14	9		30	30	
I/O	6	A13	11		31	31	
I/O	6	B12	13		32	32	
I/O	6	A12	15		33	33	
Set I/O direction Bank 5 FPGA Pin = D16 J1 controls selection of I/O termination voltage							
I/O	10	A6	17		34	34	
I/O	10	B6	19		35	35	
I/O	10	A5	21		36	36	
I/O	10	C5	23		37	37	
I/O	10	A4	25		38	38	
I/O	10	B4	27		39	39	
I/O	10	A3	29		40	40	
I/O	10	B3	31		41	41	
Set I/O direction Bank 6 FPGA Pin = H13 J1 controls selection of I/O termination voltage							
I/O	9	C11	33		42	42	
I/O	9	A11	35		43	43	
I/O	9	B10	37		44	44	
I/O	9	A10	39		45	45	
I/O	9	C9	41		46	46	
I/O	9	A9	43		47	47	
I/O	9	A7	45		48	48	
I/O	9	C7	47		49	49	
GND	-	-	49		25	25	
GND	-	-	50		50	50	

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